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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,827	12/01/2003	Charles Forbes	108-278USADA0	3586
7590	12/03/2008	Thomas J. Perkowski, Esq., PC 1266 East Main Street Stamford, CT 06902	EXAMINER	
		DHARIA, PRABODH M		
		ART UNIT		PAPER NUMBER
		2629		
		MAIL DATE		DELIVERY MODE
		12/03/2008		PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/725,827	FORBES ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	PRABODH M. DHARIA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 22 September 2008.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 43 is/are pending in the application.
- 4a) Of the above claim(s) 1-42 and 44-95 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 43 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 01 December 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ .  | 6) <input type="checkbox"/> Other: _____ .                        |

1. **Status:** Please all the replies and correspondence should be addressed to Examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 09-22-2008 under amendments, which have been placed of record in the file. Claim 43 is pending. Claims 1-42 and 44-95 are cancelled.

***Response to Amendment***

2. The amendment filed 12-01-2003 does not introduce any new matter into the disclosure. The added material is supported by the original disclosure. Applicant has cancelled claims 1-42 and 44-95 and amended claim 43 to overcome prior art rejection.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kazlas, Peter T. et al. (US 20040180476 A1) in view of Albert; Jonathan D et al. (US 6232950 B1).

Regarding Claim 43, Kazlas, Peter T. et al. (US 20040180476 A1) discloses a thin film transistor backplane (please see abstract, figure 1, page 2, paragraph 19, Line 1,2) , comprising: a polyimide substrate (page 8, paragraph 101-109); a first passivation layer deposited on a deposition surface of the polyimide substrate (page 8, paragraph 101-109, page 6, paragraph 78,

page 7, paragraph 98); an array of gate electrodes and gate lines patterned on the passivation layer (page 6, paragraph 78; page 7, paragraphs 89,90, page 8, paragraph 110) a gate insulating layer deposited over the array of gate electrodes and gate lines; a semiconducting channel layer deposited over the gate insulating layer; a contact layer deposited on and in contact with the channel layer; and an array of source electrodes, drain electrodes, lines and pads fabricated on and in contact with the contact layer (page 6, paragraph 78, 81-88; page 7, paragraphs 88-90, page 8, paragraphs 101-110, page 3, paragraph 29, pages 4,5, paragraphs 67-70, discloses basic transistor construction using polyimide substrate with passivation layer; it is well known to one ordinary skill in the art the channeling regions are formed while depositing the source regions and drain regions, and when voltage applied across the gate to turn the TFT on would have current flowing through channel between source and drain please see Wu; Chung-Cheng et al. (US 6175394 B1) please see figure 4-8, Col. 1, Lines 57-67, Col. 5, Line 50 to Col. 6, Line 56, Col. 7, Line 30 to Col. 8, Line 12).

However, Kazlas, Peter T. et al. (US 20040180476 A1) fails to disclose a thin film flexible transistor backplane for use in electronic-ink based display devices.

However, Albert; Jonathan D et al. (US 6232950 B1) discloses a thin film flexible transistor backplane (Col. 17, Line 58 to Col. 18, Line 7) for use in electronic-ink based display devices, (Col. 18, Line 43 to Col. 19, Line 21 discloses electronic ink display; please also see Col. 5, Line 63 to Col. 7, Line 17 discloses the detail description of the electronic ink display) said thin film flexible transistor backplane comprising: a polyimide substrate having a deposition surface and thickness to exhibit flexible characteristics in at least one dimension ((Col. 17, Line 58 to Col. 18, Line 7).

The reason to combine to be able to have highly flexible reflective printable display that do not require any backlighting , however, the display is reflective consumes less power and can be incorporated in a variety of application. The flexible thin film transistor backplane allows each of the display elements addressable.

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Albert; Jonathan D et al. (US 6232950 B1) in the teaching of Kazlas, Peter T. et al. (US 20040180476 A1) to be able to achieve a flat panel display using electronic in having a flexible thin film transistor backplane allows each of the display elements addressable and display is highly flexible reflective printable display that do not require any backlighting , however, the display is reflective consumes less power and can be incorporated in a variety of application with easy manufacturability and made inexpensively (Col. 1, Lines 37-40, Col. 2, Line 1-9, Col. 17, Line 58 to Col. 18, Line 7).

### ***Response to Arguments***

5. Applicant's arguments, see remark, filed 09-22-2008, with respect to amended claim(s) 43; have been fully considered and are persuasive. However, upon further consideration, a new ground(s) of rejection is made in view of Albert; Jonathan D et al. (US 6232950 B1).

### ***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PRABODH M. DHARIA whose telephone number is (571)272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

8. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 10/725,827  
Art Unit: 2629

Page 6

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

/Prabodh M Dharia/

Primary Examiner

Art Unit 2629

December 01, 2008